

**Logic4Motion** is a library of FPGA IPs implementing Field-Oriented Control (FOC) for permanent magnet, induction and stepper motors.

**Logic4Motion** features high control frequency and powerful monitoring/diagnostics support. Developed with Xilinx HLS, it is the ideal solution to take advantage of both HW power and easier, higher-level development methodology of C, compared to HW description languages.

## OVERVIEW

When an FPGA best fits your motor drive HW architecture, developing the control application in C may help you to considerably reduce design time, costs and maintenance.

Microcontrollers available today enable the design of excellent SW-based Field Oriented Control (FOC) for electric motors (synchronous permanent magnet motors, induction motors, steppers motors, etc.) cost-effective and high-performance: for example, a Cortex M3 core @120MHz can execute a fixed-point FOC algorithm achieving 50usec of cycle time or less.

However, when the system application requires multi-axis control with narrow cycle time constraints, or the integration of complex communication/monitoring tasks, as interfaces to a field bus (e.g EtherCAT), a low-cost microcontroller solution is not suitable.

Focusing on higher-level processor platforms typically leads to higher costs and complexity and still doesn't ensure to fulfill all the system requirements (i.e the management of several complex tasks with hard time constraints) with a single-processor architecture.

Multiple tasks in an FPGA (control tasks, communication tasks, etc.) may be simply managed by implementing multiple IPs instances: the constraint here is the FPGA fabric size.

Existing motor control IPs targeted to FPGA implementation are typically developed in VHDL or other HW description language: this requires specific experience and normally implies a significant complexity in terms of design development and maintenance.

**Logic4Motion** enables the design of your FOC application in C language and its direct implementation to FPGA.

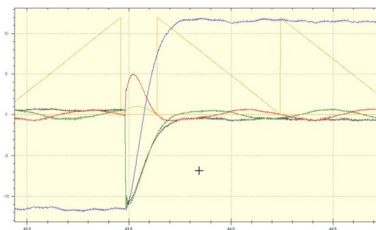
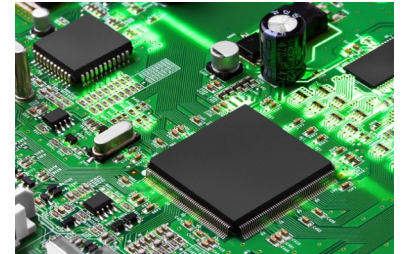
**Logic4Motion** has been developed using Xilinx HLS and is specially targeted to Xilinx ZynQ® SOC.

You can develop, update, maintain your control design in C, translate it to VHDL and implement to FPGA:  
**HW performance with SW flexibility.**

## HIGHLIGHTS

### Control algorithm in hardware

Control State-Machine calculations implemented in HW to achieve high loop-control frequency: HW performance with SW flexibility.



### Powerful monitoring & diagnostics

The integrated monitor IP performs sampling at loop-control cycle time of most relevant process variables, such as current, speed, torque, position. The PC companion tool supports downloading, visualization and analysis of data.

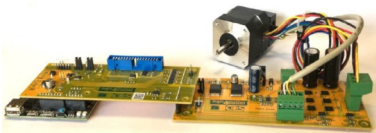
### Developed in HLS

Control algorithms, Park and Clarke transforms, current, speed and position PID controllers: all process modules developed in C language and translated to VHDL with Xilinx HLS. Outstanding small effort / short time for modification and maintenance. No VHDL skill required.

```

30 void main()
31 {
32     int i = 0;
33
34     // extract current ia and ib
35     ia = GetCurrentIa();
36     ib = GetCurrentIb();
37     // a,b,c -> alfa, beta
38     clarke();
39     // alfa, beta -> D,Q
40     park();
41     // control Q axis
42     pid_Q();
43     // control D axis
44     pid_D();
45     // control velocity
46     pid_velocity();
47     // space vector modulator
48     space_vector();
49 }
50

```



### L4M Motor control kit

L4M Motor Control Kit is a cost effective hardware platform suited for exploring logic4motion FPGA library functionality. Designed for Avnet Minized board (or every board with Arduino compatible shield connectors)

## FEATURES

- Deterministic control cycle time
- High resolution and high performance Field-Oriented Control (FOC)
- Space Vector Modulation
- Scalable solution for multi-axis control drive design
- Acquisition and visualization of internal signals for debugging, monitoring and application tuning
- FOC with Resolver or Encoder position transducer
- Cost-effective integration with custom systems or field buses that requires FPGA implementation
- Windows interface API for parameters configuration and drive monitoring
- Developed with HLS (easy maintenance, no VHDL experience required)
- Specially targeted to Xilinx Zynq® implementation
- Reference design based on AVNET MicroZed™ / ZedBoard™ and FMC motor control board